IN THE CLAIMS:

Claims 3 and 11 were previously cancelled. Claims 1 and 2 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Currently amended) A lead frame of a plurality of lead frames, the lead frame for a semiconductor device having a first surface having at least one bond pad located thereon and having a bottom surface, the lead frame comprising:

a lead frame of a plurality of lead frames, each lead frame located adjacent another lead frame having an opening located therebetween;

a plurality of lead fingers of the lead frame, each lead finger of the plurality having an end, at least a portion of the plurality of lead fingers having an opening for locating a semiconductor device therein having ~~said~~ the plurality of lead fingers located adjacent ~~the~~ to sides of the semiconductor device;

at least one bus bar having a portion extending along the end of ~~the at least one~~ each lead finger of the plurality of lead fingers and along a portion of one side of a semiconductor device when located in ~~said~~ the opening; and

a section of tape substantially rectangular in shape having an outer peripheral portion and a central portion for attaching at least a portion of the first surface of the semiconductor device thereto, the outer peripheral portion of the section of tape for attaching at least a portion of at least two ends of the lead fingers of the plurality of lead fingers thereto, the section of tape being attached to a portion of the at least one bus bar.

2. (Currently amended) The lead frame of claim 1, wherein the lead frame includes at least two bus bars, each bus bar of the at least two bus bars having a longitudinal contact portion extending along the end of ~~the at least one~~ each lead finger of the plurality of lead fingers.

3. (Cancelled)

4. (Previously Presented) A lead frame of a plurality of lead frames for connecting a semiconductor device thereto having a periphery, the lead frame comprising:

a lead frame of a plurality of lead frames, each lead frame located adjacent another lead frame having an opening therebetween;

a plurality of lead fingers of the lead frame, each lead finger of the plurality of lead fingers having an end, at least a portion of the plurality of lead fingers defining a semiconductor device opening in the lead frame;

a die paddle for supporting the semiconductor device thereon; and

at least two bus bars, each having at least a portion thereof extending along at least portions of two adjacent portions of the periphery of the semiconductor device, the at least two bus bars having a portion thereof extending along the end of the each lead finger of the plurality of lead fingers.

5. (Previously Presented) A lead frame of a plurality of lead frames for use with a semiconductor device having a periphery, the lead frame comprising:

a lead frame located adjacent another lead frame of a plurality of lead frames having an opening therebetween, the lead frame having a plurality of inwardly extending leads extending to an opening for a semiconductor device to be located therein, at least one lead of the plurality of inwardly extending leads having a portion extending along at least a portion of a length of at least two adjacent portions of the periphery of a semiconductor device and extending between the semiconductor device and another lead of the plurality of inwardly extending leads and a second inwardly extending lead extending along another portion of the length of the at least two adjacent portions of the periphery of a semiconductor device, the at least one lead of the plurality of inwardly extending leads for electrically connecting a semiconductor device to a power source.

6. (Previously Presented) The lead frame of claim 5, wherein the at least one lead of the plurality of inwardly extending leads electrically connects the semiconductor device to ground.

7. (Previously Presented) The lead frame of claim 5, wherein the at least one lead of the plurality of inwardly extending leads electrically connects the semiconductor device to a reference voltage.

8. (Previously Presented) The lead frame of claim 5, wherein the at least one lead of the plurality of inwardly extending leads substantially surrounds the at least two adjacent portions of the periphery of the semiconductor device.

9. (Previously Presented) The lead frame of claim 5, wherein the at least one lead of the plurality of inwardly extending leads is bifurcated.

10. (Previously Presented) The lead frame of claim 9, wherein a first portion of the at least one inwardly extending bifurcated lead extends along a first portion of the periphery of the semiconductor device and a second portion of the at least one inwardly extending bifurcated lead extends along another adjacent portion of the periphery of the semiconductor device.

11. (Cancelled)

12. (Previously Presented) The lead frame of claim 5, wherein the at least one lead of the plurality of inwardly extending leads extends along a portion of the periphery of the semiconductor device and the second inwardly extending lead extends along another opposite portion of the periphery of the semiconductor device.

13. (Previously Presented) The lead frame of claim 12, wherein the at least one lead of the plurality of inwardly extending leads substantially surrounds the semiconductor device and the second inwardly extending lead substantially surrounds the semiconductor device.

14. (Previously Presented) The lead frame of claim 12, wherein the at least one lead of the plurality of inwardly extending leads and the second inwardly extending lead are bifurcated forming a first portion and a second portion on the at least one lead of the plurality of inwardly extending leads and a first portion and a second portion on the second inwardly extending lead.

15. (Previously Presented) The lead frame of claim 14, wherein the first portion of the at least one bifurcated, inwardly extending lead extends along a first portion of the periphery of the semiconductor device and the second portion of the at least one bifurcated, inwardly extending lead extends along a second portion of the periphery of the semiconductor device and the first portion of the second bifurcated, inwardly extending lead extends along a third portion of the periphery of the semiconductor device and the second portion of the second bifurcated, inwardly extending lead extends along a fourth portion of the periphery of the semiconductor device.